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1 Power optimizations for cache memory: Location cache: a low-power L2 cache system

Rui Min, Wen-Ben Jone, Yiming Hu

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(406.29 KB) Additional Information: full citation, abstract, references, index terms

While set-associative caches incur fewer misses than direct-mapped caches, they typically have slower hit times and higher power consumption, when multiple tag and data banks are probed in parallel. This paper presents the location cache structure which significantly reduces the power consumption for large set-associative caches. We propose to use a small cache, called *location cache* to store the location of future cache references. If there is a hit in the location cache, the supported c ...

Keywords: L1/L2 caches, TLB, data location, power, set-associative caches

2 Power supply, voltage, and frequency management: Maximizing efficiency of solar-powered systems by load matching

Dexin Li, Pai H. Chou

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(3.19 MB) Additional Information: full citation, abstract, references, index terms

Solar power is an important source of renewable energy for many low-power systems. Matching the power consumption level with the supply level can make a great difference in the efficiency of power utilization. This paper proposes a source-tracking power management strategy that maximizes the panel's total energy output under a given solar profile by load matching. The power efficiency was validated by extensive measurement. Compared to a conventional solar powered system, our load matching strat ...

Keywords: load matching, photovoltaics, power management, power model, solar energy, solar-aware

3 Wireless application drivers for low-power systems: FSM--based power modeling of wireless protocols: the case of bluetooth

Luca Negri, Mariagiovanna Sami, David Macii, Alessandra Terranegra

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(258.49 KB) Additional Information: full citation, abstract, references, index terms

The proliferation of pervasive computing applications relying on battery--powered devices and wireless connectivity is posing great emphasis on the issue of power optimization. While node--level models and approaches have been widely discussed, a problem requiring even greater attention is that of power associated with the communication protocols. We propose a high--level modeling methodology based on Finite State Machines useful to predict the energy consumption of given communication tasks wit ...

Keywords: bluetooth, power modeling, wireless protocols

4 Modeling and simulating electronic textile applications

Thomas Martin, Mark Jones, Joshua Edmison, Tanwir Sheikh, Zahi Nakad

June 2004 **ACM SIGPLAN Notices , Proceedings of the 2004 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools**, Volume 39 Issue 7

Full text available: pdf(421.80 KB) Additional Information: full citation, abstract, references, index terms

This paper describes our design of a simulation environment for electronic textiles (e-textiles) and our experiences with that environment. This simulation environment, based upon Ptolemy II, enables us to model a diverse range of areas related to the design of electronic textiles, including the physical environment they will be used in, the behavior of the sensors incorporated into the fabric, the on-fabric network, the power consumption of the system, and the execution of the application and s ...

Keywords: context awareness, electronic textiles, smart fabrics, wearable computing

5 Interconnect extraction: CHIME: coupled hierarchical inductance model evaluation

Satrajit Gupta, Lawrence T. Pileggi

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(167.77 KB) Additional Information: full citation, abstract, references, index terms

Modeling inductive effects accurately and efficiently is a critical necessity for design verification of high performance integrated systems. While several techniques have been suggested to address this problem, they are mostly based on sparsification schemes for the L or L-inverse matrix. In this paper, we introduce CHIME, a methodology for non-local inductance modeling and simulation. CHIME is based on a hierarchical model of inductance that accounts for all inductive couplings at a linear cos ...

Keywords: circuit simulation, inductance modeling

6 Numerical techniques for simulation: A frequency relaxation approach for analog/RF system-level simulation

Xin Li, Yang Xu, Peng Li, Padmini Gopalakrishnan, Lawrence T. Pileggi

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(191.49 KB) Additional Information: full citation, abstract, references, index terms

The increasing complexity of today's mixed-signal integrated circuits necessitates both top-down and bottom-up system-level verification. Time-domain state-space modeling and simulation approaches have been successfully applied for such purposes (e.g. Simulink); however, analog circuits are often best analyzed in the frequency domain. Circuit-level analyses, such as harmonic balance, have been successfully extended to the frequency domain [2], but these algorithms are impractical for simulating ...

Keyw rds: analog/RF circuits, system-level simulation

7 New technologies in system design: Performance analysis of different arbitration algorithms of the AMBA AHB bus

Massimo Conti, Marco Caldari, Giovanni B. Vece, Simone Orcioni, Claudio Turchetti
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(200.79 KB) Additional Information: full citation, abstract, references, index terms

Bus performances are extremely important in a platform-based design. System Level analysis of bus performances gives important information for the analysis and choice between different architectures driven by functional, timing and power constraints of the System-on-Chip. This paper presents the effect of different arbitration algorithms and bus usage methodologies on the bus AMBA AHB performances in terms of effective throughput and power dissipation. SystemC and VHDL models have been developed ...

Keywords: AMBA AHB BUS, arbitration algorithm, performance, systemC

8 Optimization: High-speed, scalable, real-time simulation using DSP arrays

Roy Crosbie, John Zenor, Richard Bednar, Dale Word, Narain Hingorani, Terry Ericsen
May 2004 **Proceedings of the eighteenth workshop on Parallel and distributed simulation**

Full text available: pdf(156.87 KB) Additional Information: full citation, abstract, references

Real-time simulation is a familiar technique for testing hardware and software in the loop and for operator training. An important parameter of these simulations is the frame-time necessary to capture the dynamics of the system being simulated. Modern power electronic systems, using higher frequency pulse-width modulation (PWM) converter control demand frame times that are significantly shorter than those found in most real-time simulators. The paper describes an approach to real-time simulation ...

9 Oral presentation session 1: In network modeling, processing, & optimization: Entropy-based sensor selection heuristic for target localization

Hanbiao Wang, Kung Yao, Greg Pottie, Deborah Estrin
April 2004 **Proceedings of the third international symposium on Information processing in sensor networks**

Full text available: pdf(270.37 KB) Additional Information: full citation, abstract, references, index terms

We propose an entropy-based sensor selection heuristic for localization. Given 1) a prior probability distribution of the target location, and 2) the locations and the sensing models of a set of candidate sensors for selection, the heuristic selects an informative sensor such that the fusion of the selected sensor observation with the prior target location distribution would yield on average the greatest or nearly the greatest reduction in the entropy of the target location distribution. The heu ...

Keywords: Shannon entropy, information fusion, information-directed resource management, mutual information, sensor selection, target localization, target tracking, wireless sensor networks

10 (Special session) invited talks: selected European activities in SoC low power design methodologies and research networking: Predictable design of low power systems by pre-implementation estimation and optimization

Wolfgang Nebel

January 2004 **Pr ceedings f the 2004 conference n Asia S uth Pacific design aut mation: electr nic design and s luti n fair 2004**

Full text available: pdf(185.22 KB) Additional Information: full citation, abstract, references

Each year tens of billions of Dollars are wasted by the microelectronics industry because of missed deadlines and delayed design projects. These delays are partially due to design iterations many of which could have been avoided if the low level remifications of high level design decisions, at the Architecture- and Algorithmic-level would have been known before the time consuming and tedious RT- and lower level implementation started. In this contribution we present a System-level design flow an ...

11 Integrating biopathway databases for large-scale modeling and simulation

Masao Nagasaki, Atsushi Doi, Hiroshi Matsuno, Satoru Miyano

January 2004 **Proceedings of the second conference on Asia-Pacific bioinformatics - Volume 29**

Full text available: pdf(692.38 KB) Additional Information: full citation, abstract, references

Biopathway databases have been developed, such as KEGG and EcoCyc, that compile interaction structures of biopathways together with biological annotations. However, these biopathways are not directly editable and simulatable. Thus, we have made an application, the Biopathway Executer (BPE), that reconstructs these two major biopathway databases to XML formats of modeling and simulation platforms. BPE is developed with JAVA and has a database of executable biopathways that integrates some parts o ...

Keywords: Genomic Object Net, Petrinet, biopathways, database, pathway modeling, simulation

12 Single-ISA Heterogeneous Multi-Core Architectures: The Potential for Processor Power Reduction

Rakesh Kumar, Keith I. Farkas, Norman P. Jouppi, Parthasarathy Ranganathan, Dean M. Tullsen

December 2003 **Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture**

Full text available: pdf(295.12 KB) Publisher Site Additional Information: full citation, abstract, index terms

This paper proposes and evaluates single-ISA heterogeneousmulti-core architectures as a mechanism to reduceprocessor power dissipation. Our design incorporatesheterogeneous cores representing different points inthe power/performance design space; during an application'sexecution, system software dynamically chooses themost appropriate core to meet specific performance andpower requirements.Our evaluation of this architecture shows significant energybenefits. For an objective function that optimi ...

13 Dynamic Fault-Tolerance and Metrics for Battery Powered, Failure-Prone Systems

Phillip Stanley-Marbell, Diana Marculescu

November 2003 **Proceedings of the 2003 international conference on on Computer-aided design**

Full text available: pdf(496.57 KB) Additional Information: full citation, abstract

Emerging VLSI technologies and platforms are giving rise tosystems with inherently high potential for runtime failure.Such failures range from intermittent electrical and mechanicalfailures at the system level, to device failures at the chip level.Techniques to provide reliable computation in the presence offailures must do so while maintaining high performance, withan eye toward energy efficiency. When possible, they shouldmaximize battery lifetime in the face of battery discharge non-lineariti ...

14 Case studies in embedded systems: The analysis and design of architecture systems for speech recognition on modern handheld-computing devices

Andreas Hagen, Daniel A. Connors, Bryan L. Pellom

October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

Full text available: pdf(280.91 KB) Additional Information: full citation, abstract, references, index terms

Growing demand for high performance in embedded systems is creating new opportunities to use speech recognition systems traditionally executed only on high performance systems. In several ways, the needs of embedded computing differ from those of more traditional general-purpose systems. Embedded systems have more stringent constraints on cost and power consumption that lead to design bottlenecks for many computationally-intensive applications. This paper characterizes the speech recognition pro ...

Keywords: embedded systems, performance, speech recognition

15 Engineering of markets and artifacts

Eswaran Subrahmanian, Sarosh N. Talukdar

September 2003 **Proceedings of the 5th international conference on Electronic commerce**

Full text available: pdf(109.77 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we continue the dialog started by Roth [19] between economics and engineering in the context of design of markets. We take the position that markets and engineered artifacts are thee the products of a social process of design formulation. Our perspective is that designing of markets and artifacts follow the same kind of problem formulation and solution testing process. Further, we show through two case studies, that the design of engineered artifacts and markets are often interdep ...

Keywords: engineering design, market design, methodologies, modeling, testing

16 System estimation and voltage scheduling: B#: a battery emulator and power profiling instrument

Pai H. Chou, Chulsung Park, Jae Park, Kien Pham, Jinfeng Liu

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(499.16 KB) Additional Information: full citation, abstract, references, index terms

This paper describes B# (B-sharp), a programmable power supply that emulates the behavior of a battery. It measures the current load, calls a battery simulation program to compute the voltage in real time, and controls a linear regulator to mimic the voltage output of a battery. This instrument enables validation of battery-aware power-optimization techniques with accurate, controllable, reproducible results. This instrument also supports training mode with actual batteries, and it can even be u ...

Keywords: battery emulation, power profiling instrument

17 Temperature and power aware architectures: Reducing power density through activity migration

Seongmoo Heo, Kenneth Barr, Krste Asanović

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(144.76 KB) Additional Information: full citation, abstract, references, citings, index

terms

Power dissipation is unevenly distributed in modern microprocessors leading to localized hot spots with significantly greater die temperature than surrounding cooler regions. Excessive junction temperature reduces reliability and can lead to catastrophic failure. We examine the use of activity migration which reduces peak junction temperature by moving computation between multiple replicated units. Using a thermal model that includes the temperature dependence of leakage power, we show that sust ...

Keywords: activity migration, temperature reduction, thermal model

18 Design strategies for controlling standby leakage: Design methodology for fine-grained leakage control in MTCMOS

Benton H. Calhoun, Frank A. Honore, Anantha Chandrakasan

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(197.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Multi-threshold CMOS is a popular technique for reducing standby leakage power with low delay overhead. MTCMOS designs typically use large sleep devices to reduce standby leakage at the block level. We provide a formal examination of sneak leakage paths and a design methodology that enables gate-level insertion of sleep devices for sequential and combinational circuits. A fabricated 0.13 µm, dual V T testchip employs this methodology to implement a low-power FPGA core with gate-level sleep ...

Keywords: MTCMOS, circuit design, design methodology, fine-grain sleep regions, leakage, low power, sleep mode, sneak leakage

19 The *n*-hop multilateration primitive for node localization problems

Andreas Savvides, Heemin Park, Mani B. Srivastava

August 2003 **Mobile Networks and Applications**, Volume 8 Issue 4

Full text available: pdf(208.39 KB) Additional Information: full citation, abstract, references, index terms

The recent advances in MEMS, embedded systems and wireless communication technologies are making the realization and deployment of networked wireless microsensors a tangible task. In this paper we study node localization, a component technology that would enhance the effectiveness and capabilities of this new class of networks. The *n*-hop multilateration primitive presented here, enables ad-hoc deployed sensor nodes to accurately estimate their locations by using known beacon locations tha ...

Keywords: ad-hoc localization, distributed localization, sensor networks

20 Energy management for battery-powered embedded systems

Daler Rakhmatov, Sarma Vrudhula

August 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 3

Full text available: pdf(603.41 KB) Additional Information: full citation, abstract, references, citings, index terms

Portable embedded computing systems require energy autonomy. This is achieved by batteries serving as a dedicated energy source. The requirement of portability places severe restrictions on size and weight, which in turn limits the amount of energy that is continuously available to maintain system operability. For these reasons, efficient energy utilization has become one of the key challenges to the designer of battery-powered

embedded computing systems.In this paper, we first present a novel a ...

Keyw rds: Battery, low-power design, modeling, scheduling, voltage scaling

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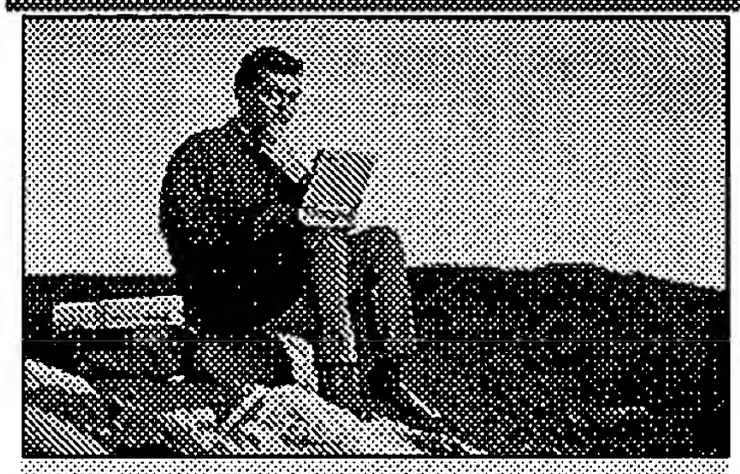

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